

Ethernet MAC

10 / 100 / 1000 Mbps hardware Media Access Controller

• FPGA-PROVEN

Product code: NSN-NET-EMAC · Implemented in C₊₊ · Source-included · Verilog / VHDL output

The Neosyn Ethernet MAC is a complete IEEE 802.3 Media Access Control layer realised entirely in hardware — no embedded processor and no firmware. It supports full-duplex operation at 10, 100 and 1000 Mbps over a standard MII/GMII PHY interface, with auto-negotiation, an integrated receive buffer, and on-the-fly filtering of malformed frames.

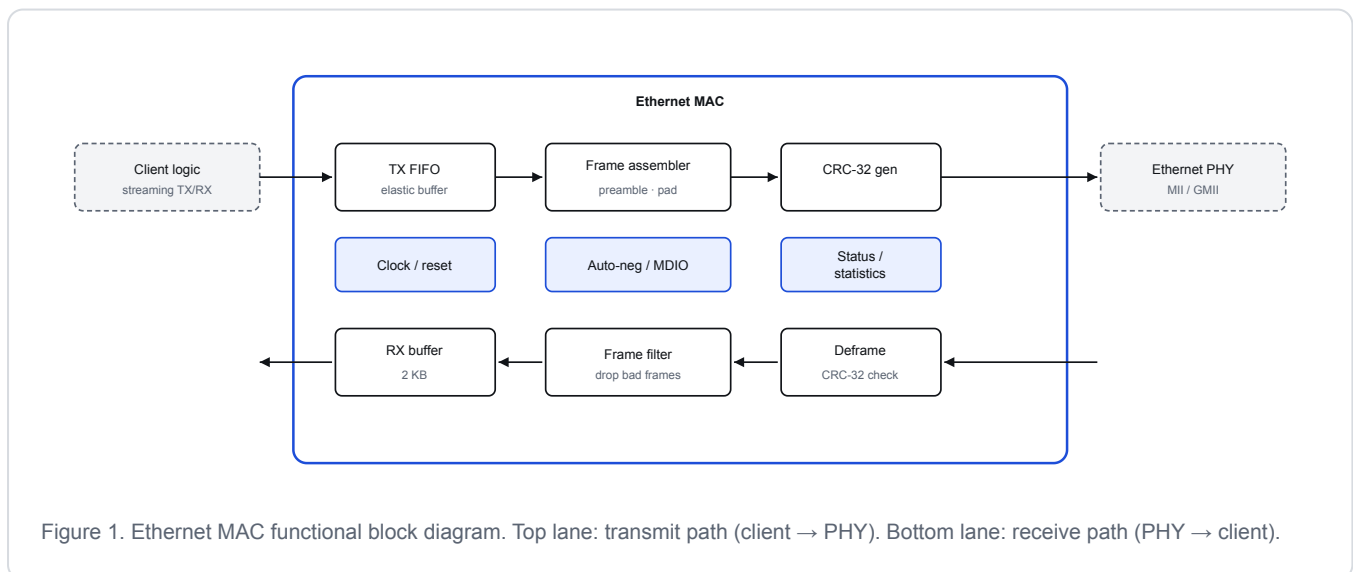
The core presents a simple streaming interface to the client logic, so user designs send and receive Ethernet frames without managing the PHY handshake, preamble, padding or CRC. It is silicon-proven on a Lattice ECP3 platform with a Marvell PHY and has already been licensed into a shipping product.

Because the core is written in C₊₊ and shipped with source, the generated Verilog is fully reviewable and the design is straightforward to audit, retarget and customise — unlike an encrypted netlist.

KEY FEATURES

- Full-duplex 10/100/1000 Mbps
- 100% hardware — no CPU/firmware
- MII & GMII PHY interface
- Clause-28 auto-negotiation
- 2 KB receive buffer
- Bad-frame filtering (preamble / length / CRC)
- Streaming client interface
- Vendor-independent RTL
- Source-included (C₊₊ + HDL)

— Architecture



1 Overview

The Ethernet MAC implements the data-link MAC sublayer of IEEE 802.3. On transmit it accepts a payload from the client, assembles a valid Ethernet frame (preamble, start-of-frame delimiter, padding to the minimum frame size) and appends a 32-bit CRC before driving the PHY. On receive it recovers frames from the PHY, validates the CRC and frame structure, discards malformed frames, and buffers valid frames for the client.

All control is in hardware: there is no soft CPU, no driver and no firmware in the data path. This makes the core deterministic and suitable for systems where a processor is unavailable or undesirable, and where wire-speed throughput at low, fixed latency is required.

2 Features

- **Line rates.** Full-duplex 10, 100 and 1000 Mbps, selectable via auto-negotiation or fixed configuration.
- **PHY interface.** Media-Independent Interface (MII) and Gigabit MII (GMII).
- **Auto-negotiation.** IEEE 802.3 Clause 28 negotiation of speed and duplex with the link partner.
- **Frame processing.** Automatic preamble/SFD insertion, padding to 64-byte minimum, and CRC-32 generation on transmit; CRC and structural checking on receive.
- **Receive buffering.** Integrated 2 KB receive buffer absorbing client back-pressure.
- **Frame filtering.** Drops frames with a missing preamble, length errors, or a bad CRC before they reach the client.
- **Client interface.** Simple streaming send/receive — the client never touches the PHY handshake.
- **Portability.** Vendor-independent RTL generated from C₊₊; targets Intel, AMD/Xilinx, Lattice and Microchip, or an open-source flow.

3 Functional description

Refer to Figure 1. The MAC is organised as independent transmit and receive paths with shared auto-negotiation/management and clock/reset logic.

3.1 Transmit path

Client payload is written into an elastic **TX FIFO** that decouples the client clock domain from the PHY transmit clock. The **frame assembler** prepends the preamble and start-of-frame delimiter and pads short payloads to the 64-byte minimum frame length. The **CRC-32 generator** computes and appends the frame check sequence. The completed frame is presented to the PHY across the MII/GMII transmit interface.

3.2 Receive path

Frames arriving from the PHY are de-framed: the preamble/SFD are stripped and the **CRC-32 check** validates the frame check sequence. The **frame filter** discards frames that are malformed — missing preamble, length out of range, or failing CRC — so only valid frames consume buffer space. Valid frames are written to the **2 KB receive buffer** and handed to the client through the streaming interface.

3.3 Auto-negotiation & management

The auto-negotiation/MDIO block negotiates speed and duplex with the link partner per Clause 28 and provides management access to the PHY. Fixed-mode operation is also supported where negotiation is not desired.

Note. The core is silicon-proven on a Lattice ECP3 Versa development board paired with a Marvell 88E1119R PHY. It is not limited to that combination; any compliant MII/GMII PHY is supported.

4 Interfaces & signals

The core exposes three groups of signals: the PHY-side MII/GMII interface, the client-side streaming interface, and clock/reset. Exact port names are provided with the deliverable; the table below summarises the interface groups.

GROUP	DIRECTION	DESCRIPTION
GMII/MII TX	MAC → PHY	Transmit data + control to the PHY (data, enable, error), TX clock.
GMII/MII RX	PHY → MAC	Receive data + control from the PHY (data, valid, error), RX clock.
MDIO	bidirectional	PHY management / auto-negotiation control.
Client TX	client → MAC	Streaming payload in, with handshake/back-pressure.
Client RX	MAC → client	Streaming payload out, with handshake/back-pressure.
Clock / reset	in	MAC clock domain and synchronous reset; PHY-derived clocks.

Detailed signal-level pinout (per-bit widths, polarities, timing) is available on request and ships with the core.

5 Protocol & standards compliance

ITEM	DETAIL
MAC sublayer	IEEE 802.3 framing (preamble, SFD, length/type, payload, padding, FCS)
PHY interface	MII (10/100) and GMII (1000) media-independent interfaces
Auto-negotiation	IEEE 802.3 Clause 28 (speed + duplex)
Frame check	32-bit CRC (FCS) generation on TX, verification on RX
Duplex	Full-duplex
Min/max frame	64-byte minimum (auto-padded); standard Ethernet framing

6 Performance

PARAMETER	VALUE	NOTES
Line rate	10 / 100 / 1000 Mbps	full-duplex
Throughput	Wire-speed	line-rate; no CPU bottleneck
Receive buffer	2 KB	absorbs client back-pressure
Latency	Available on request	per configuration / target
Max clock (f_{MAX})	Available on request	per target device

7 Resource utilization

Representative utilization figures per target FPGA family are provided on request from current synthesis reports. The template below indicates the reported metrics.

TARGET FAMILY	LUTS / CELLS	REGISTERS	BLOCK RAM	F _{MAX}
Lattice ECP3	on request	on request	on request	on request
AMD/Xilinx 7-series	on request	on request	on request	on request
Intel Cyclone	on request	on request	on request	on request

Figures are supplied per project from characterised synthesis runs to avoid quoting unverified numbers.

8 Verification & validation

- Hardware-validated on a Lattice ECP3 Versa board with a Marvell 88E1119R PHY.
- Brought up against real link partners (auto-negotiation, full-duplex operation).
- Bad-frame filtering exercised across preamble, length and CRC error cases.
- Licensed into a shipping product — proven in a deployed system.

9 Deliverables

- C₊₊ source for the core (readable, modifiable).
- Generated synthesizable Verilog (VHDL on request).
- Self-checking testbench.
- Signal-level integration guide and this datasheet.
- Email integration support per the licensed tier.

10 Ordering & licensing

ITEM	DETAIL
Product code	NSN-NET-EMAC
License	Single-project or perpetual; full C ₊₊ source included
Pricing	Quoted per use (project, volume, support tier) — contact Neosyn
Support	Email integration support; custom development available
Contact	neosyn.io/contact · info@neosyn.io

11 Revision history

REV	DATE	CHANGE
A	2026	Preliminary datasheet (Neosyn / C ₁ release).

Disclaimer. This document is preliminary and provided for information only. Specifications, features and figures are subject to change without notice. Resource, timing and latency figures marked “available on request” are supplied per target device from characterised synthesis reports. The IP core is licensed, not sold, and is described as hardware; it is not certified for safety- or life-critical use and is used at the licensee’s own risk. All trademarks (IEEE, Lattice, Marvell, AMD/Xilinx, Intel, Microchip) are the property of their respective owners and are referenced for descriptive purposes only. © 2026 Neosyn. All rights reserved.