Neosyn · IP Core

DATASHEET · REV A (PRELIMINARY)

Intel 8088

8088-compatible processor core (real-mode subset)

○ AVAILABLE

Product code: NSN-CPU-8088 · Implemented in C⏚ · Source-included · Verilog / VHDL output

The Neosyn Intel 8088 core is a partial implementation of the classic 8088 processor in C⏚ — a clean, readable CPU aimed at retro-computing and retro-gaming builds, and at teaching processor and datapath design.

It implements a real-mode subset of the 8088 instruction set over an 8088-style memory bus. The C⏚ source is fully traceable, making it a strong vehicle for understanding how a CPU is built.

The core also serves as a reference processor in the Neosyn regression suite.

KEY FEATURES

- Partial 8088 ISA
- Real-mode subset
- 8088-style bus
- Retro & education
- Readable C⏚
- Vendor-independent RTL
- Source-included

— Architecture

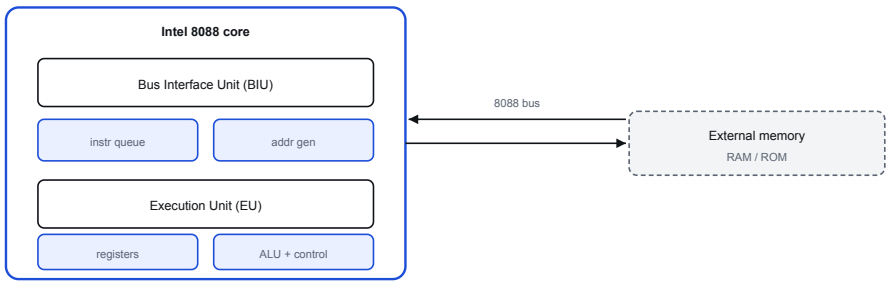

Figure 1. Intel 8088 core organisation — a Bus Interface Unit (instruction queue, address generation) and an Execution Unit (registers, ALU, control), communicating with external memory over an 8088-style bus.

1 Overview

The core implements a real-mode subset of the Intel 8088 instruction set. It is organised, in the spirit of the original, around a Bus Interface Unit that handles memory access and instruction prefetch and an Execution Unit that decodes and executes instructions over the register file and ALU.

It is intended for retro-computing and education rather than as a cycle-exact reproduction of the original part.

2 Features

- **ISA.** Partial 8088 instruction set — a real-mode subset (see the accompanying manual for coverage).
- **Bus.** 8088-style external memory bus to RAM/ROM.
- **Use cases.** Retro-computing / retro-gaming builds; processor-design education.
- **Readable.** Traceable C⏚ source — follow exactly how the CPU works.
- **Portability.** Vendor-independent RTL generated from C⏚.

3 Functional description

Refer to Figure 1.

3.1 Bus Interface Unit

The BIU drives the external memory bus, generates addresses, and prefetches instructions into a queue for the Execution Unit.

3.2 Execution Unit

The EU decodes queued instructions and executes them over the register file and ALU, writing results back and producing memory accesses via the BIU.

3.3 Coverage

A real-mode subset of the instruction set is implemented. The accompanying manual documents the supported instructions.

> **Note.** This is a partial, educational/retro implementation — not a cycle-exact reproduction of the original 8088. Instruction coverage is documented with the deliverable.

4 Interfaces & signals

The core connects to external memory over an 8088-style bus.

GROUP	DIRECTION	DESCRIPTION
Memory bus	bidirectional	8088-style address/data bus to RAM/ROM
Control	in/out	Bus control / status
Clock / reset	in	Core clock domain and synchronous reset

Detailed signal-level pinout (per-bit widths, polarities, timing) is available on request and ships with the core.

5 ISA & compatibility

ITEM	DETAIL
ISA	Intel 8088 (partial, real-mode subset)
Bus	8088-style memory bus
Mode	Real mode
Coverage	Documented subset (see manual)

6 Performance

PARAMETER	VALUE	NOTES
ISA coverage	Partial real-mode subset	see manual
Cycle accuracy	Not cycle-exact	educational/retro
Max clock (f_{MAX})	Available on request	per target device

7 Resource utilization

Representative utilization per target FPGA family is provided on request from current synthesis reports.

TARGET FAMILY	LUTS / CELLS	REGISTERS	BLOCK RAM	F_{MAX}
Lattice ECP3	on request	on request	on request	on request
AMD/Xilinx 7-series	on request	on request	on request	on request
Intel Cyclone	on request	on request	on request	on request

Figures are supplied per project from characterised synthesis runs to avoid quoting unverified numbers.

8 Verification & validation

- Instruction-level test suite.
- Runs demonstration programs (e.g. iterative Fibonacci) end to end.
- Used as a reference processor in the Neosyn regression suite.

9 Deliverables

- C⏚ source for the core (readable, modifiable)
- Generated synthesizable Verilog (VHDL on request)
- Self-checking testbench
- Integration guide and this datasheet
- Email integration support per the licensed tier

10 Ordering & licensing

ITEM	DETAIL
Product code	NSN-CPU-8088
License	Single-project or perpetual; full C⏚ source included
Pricing	Quoted per use (project, volume, support tier) — contact Neosyn
Support	Email integration support; custom development available
Contact	neosyn.io/contact · info@neosyn.io

11 Revision history

REV	DATE	CHANGE
A	2026	Preliminary datasheet (Neosyn / C⏚ release).