

UDP / IP Stack

Hardware UDP/IPv4 datagram engine

• **FPGA-PROVEN**

Product code: NSN-NET-UDPIP · Implemented in C₊₊ · Source-included · Verilog / VHDL output

The Neosyn UDP/IP Stack is a hardware implementation of the UDP-over-IPv4 protocol stack for embedded networking, with no embedded processor in the data path. It sits on top of the Neosyn Ethernet MAC to provide addressed datagram transmit and receive at line rate.

The client sends and receives UDP payloads through a simple streaming interface; the core builds and parses the UDP and IPv4 headers, manages addressing and checksums, and hands frames to the MAC. It is silicon-proven on the same Lattice ECP3 platform.

Written in C₊₊ and shipped with source, the generated RTL is fully reviewable and straightforward to retarget and customise.

KEY FEATURES

- Full-duplex 10/100/1000 Mbps
- 100% hardware — no CPU
- UDP over IPv4
- Configurable IP / port
- 2 KB receive buffer
- Bad-frame filtering
- Pairs with the Ethernet MAC
- Source-included

— Architecture

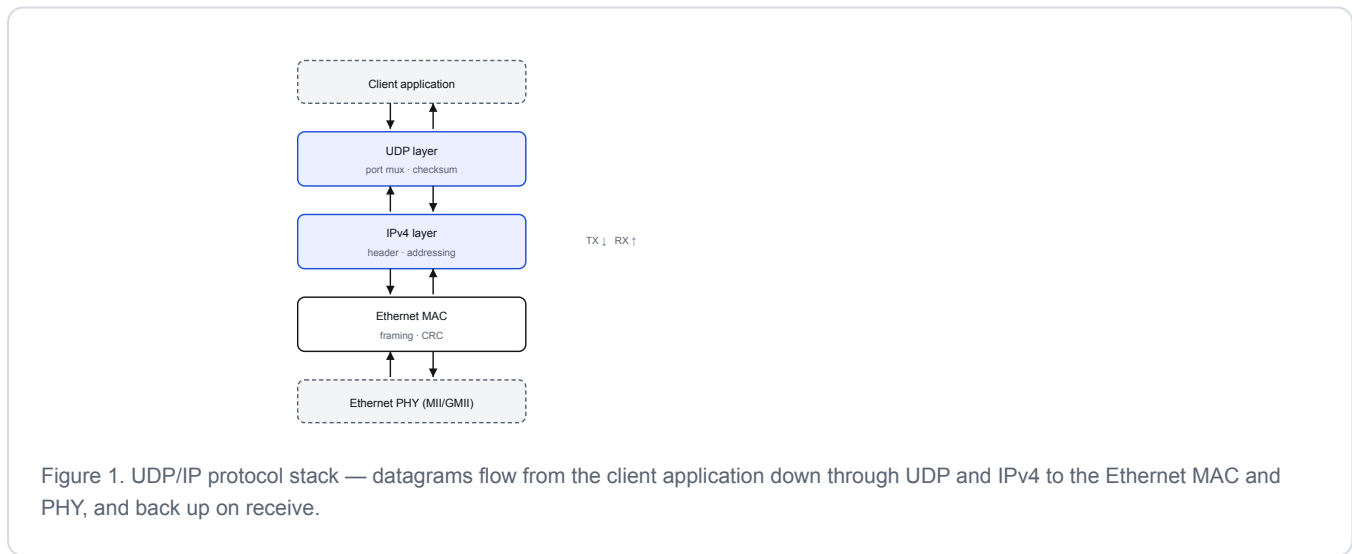


Figure 1. UDP/IP protocol stack — datagrams flow from the client application down through UDP and IPv4 to the Ethernet MAC and PHY, and back up on receive.

1 Overview

The core implements UDP (RFC 768) over IPv4. On transmit it encapsulates the client payload in a UDP datagram and an IPv4 packet, computing the required checksums, and passes the result to the Ethernet MAC. On receive it parses incoming packets, validates them, demultiplexes by UDP port, and delivers the payload to the client.

The entire stack runs in hardware with deterministic, low, fixed latency and no driver or firmware.

2 Features

- **Transport.** UDP (RFC 768) datagram encapsulation and de-encapsulation, with port multiplexing/demultiplexing.
- **Network.** IPv4 header construction and parsing; configurable source IP and destination addressing.
- **Integrity.** Header/transport checksums computed and verified in hardware.
- **Buffering & filtering.** Integrated 2 KB receive buffer; malformed frames dropped (inherited from the MAC).
- **Line rates.** Full-duplex 10/100/1000 Mbps over an MII/GMII PHY.
- **Portability.** Vendor-independent RTL generated from C₊₊; pairs with the Neosyn Ethernet MAC.

3 Functional description

Refer to Figure 1.

3.1 Transmit path

The client writes a UDP payload through the streaming interface. The UDP layer prepends the source/destination ports, length and checksum; the IPv4 layer prepends the IPv4 header and addressing. The packet is handed to the Ethernet MAC for framing and CRC.

3.2 Receive path

Incoming frames are validated by the MAC, then the IPv4 layer parses and checks the packet and the UDP layer demultiplexes by destination port. The payload is delivered to the client; non-matching or malformed packets are discarded.

3.3 Configuration

Source IP and port assignments are configurable. The stack is designed to operate directly above the Neosyn Ethernet MAC.

Note. Silicon-proven on a Lattice ECP3 Versa board with a Marvell 88E1119R PHY, on the same platform as the Ethernet MAC.

4 Interfaces & signals

The core presents a streaming application interface upward and connects to the Ethernet MAC downward.

GROUP	DIRECTION	DESCRIPTION
Application TX	client → core	UDP payload in, with handshake/back-pressure
Application RX	core → client	UDP payload out, with handshake/back-pressure
MAC interface	bidirectional	Connection to the Neosyn Ethernet MAC
Configuration	in	Source IP / port settings
Clock / reset	in	Core clock domain and synchronous reset

Detailed signal-level pinout (per-bit widths, polarities, timing) is available on request and ships with the core.

5 Protocol & standards compliance

ITEM	DETAIL
Transport	UDP — RFC 768
Network	IPv4
Link	IEEE 802.3 (via the Ethernet MAC)
Checksums	IPv4 header + UDP checksum in hardware
Addressing	Configurable source IP / port

6 Performance

PARAMETER	VALUE	NOTES
Line rate	10 / 100 / 1000 Mbps	full-duplex
Throughput	Wire-speed datagrams	no CPU bottleneck
Receive buffer	2 KB	inherited from the MAC
Latency	Available on request	per configuration

7 Resource utilization

Representative utilization per target FPGA family is provided on request from current synthesis reports.

TARGET FAMILY	LUTS / CELLS	REGISTERS	BLOCK RAM	F _{MAX}
Lattice ECP3	on request	on request	on request	on request
AMD/Xilinx 7-series	on request	on request	on request	on request
Intel Cyclone	on request	on request	on request	on request

Figures are supplied per project from characterised synthesis runs to avoid quoting unverified numbers.

8 Verification & validation

- Hardware-validated on Lattice ECP3 Versa with a Marvell 88E1119R PHY.
- Datagram send/receive validated against standard hosts.
- Operates above the proven Neosyn Ethernet MAC.

9 Deliverables

- C₊₊ source for the core (readable, modifiable)
- Generated synthesizable Verilog (VHDL on request)
- Self-checking testbench
- Integration guide and this datasheet
- Email integration support per the licensed tier

10 Ordering & licensing

ITEM	DETAIL
Product code	NSN-NET-UDPIP
License	Single-project or perpetual; full C ₊₊ source included
Pricing	Quoted per use (project, volume, support tier) — contact Neosyn
Support	Email integration support; custom development available
Contact	neosyn.io/contact · info@neosyn.io

11 Revision history

REV	DATE	CHANGE
A	2026	Preliminary datasheet (Neosyn / C ₁ release).

Disclaimer. This document is preliminary and provided for information only. Specifications, features and figures are subject to change without notice. Resource, timing and latency figures marked “available on request” are supplied per target device from characterised synthesis reports. The IP core is licensed, not sold, and is described as hardware; it is not certified for safety- or life-critical use and is used at the licensee’s own risk. All trademarks are the property of their respective owners and are referenced for descriptive purposes only. © 2026 Neosyn. All rights reserved.